AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph starting on page 7, lines 19 to 32, and continuing on page 8, lines 1-2, as follows:

Furthermore, the gate depletion effect in polycrystalline silicon gates becomes very important for ultra-thin gate insulators of logic transistors. Indeed, if the gate electrode doping level is around 10^{20} /cm^3, the depletion layer in a doped gate electrode is approximately 10 - 11 Angstroms. This would effectively thicken the ~~ultra-this~~ ultra-thin gate dielectric by 3 - 4 Angstroms of equivalent oxide thickness (EOT). With the state of the art gate insulator of 12 - 15 Angstroms, the depletion layer can degrade the performance by 20% - 30%. Therefore, it is highly desirable to increase the gate electrode doping of logic transistors to the range of $5x10^{20}$/cm^3 to $2x10^{21}$/cm^3. Such high doping levels are not required (and, hence, not used) in the memory access transistors.

Please amend the paragraph on page 19, lines 14 to 24, as follows:

Referring now to Figure 6, resist 58 is removed and the thick polisilicon 52 is etched from the array region, forming recesses 65, preferably by a process selective to nitride liner 56, which thus functions as a hard mask, and oxide 54. This takes the state of the array structure substantially to the state shown in Figure 4A while layers 52, 54 and 56 remain in the logic support area as shown in Figure 6B. In other words, at this point, the surface of the array and logic/support areas with recesses are indicated by arrow or bracket 65, respectively.